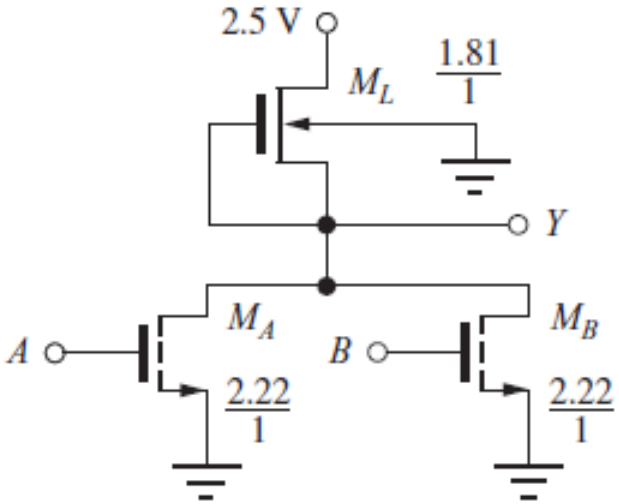
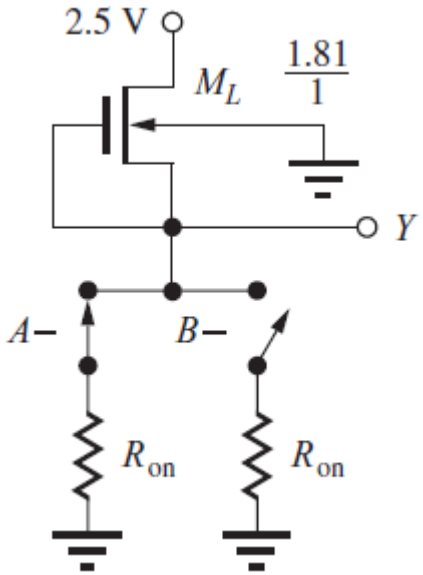
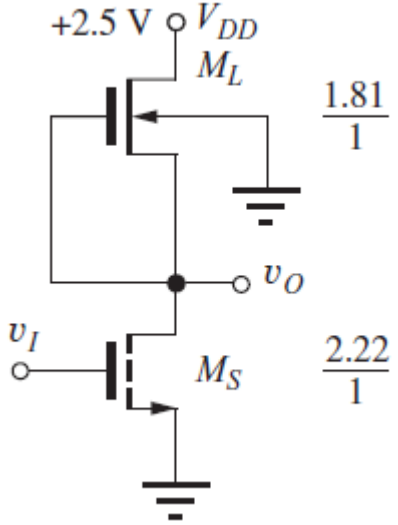
Announcements

- Exam 2 in class on Monday 5/19.
  - Example exam to be posted..

NMOS Logic Gates



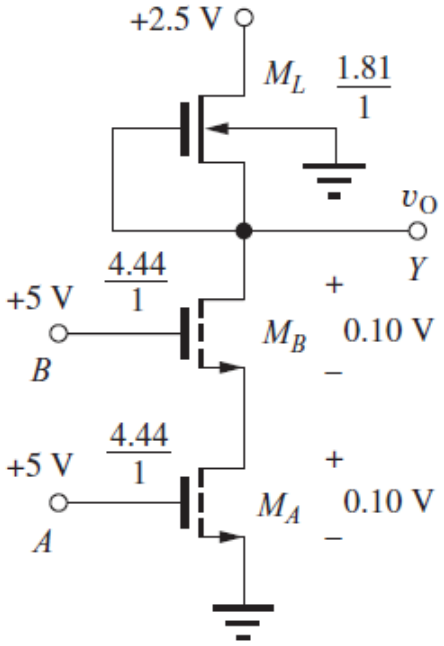


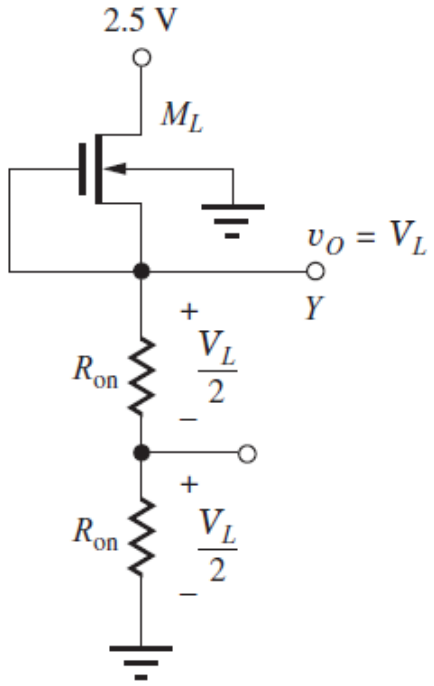


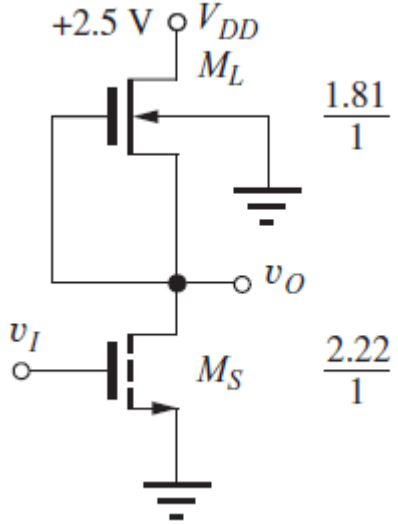
Reference inverter

- NMOS NOR Gate
  - M_A and M_B are in parallel
  - *Either* of A, B is 1, current path exists, output is 0
  - W/L same as reference inverter (to achieve the same V_L)

NMOS Logic Gates







Reference inverter

- NMOS NAND Gate
  - M_A and M_B are in series
  - Only when *both* A, B is 1, current path exists, output is 0
  - W/L doubled from reference inverter (to achieve the same V_L)

Ignore Body Effect!

Announcements

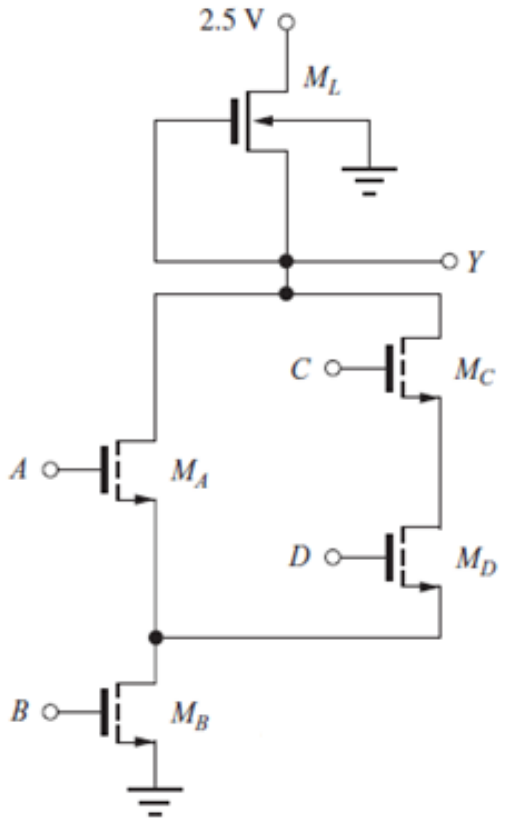
- Exam 2 in class on Monday 5/14.
  - Example exam is posted (solutions over weekend).
  - Review session, Sunday 5/13 at 5pm in EE403.
  - Need to know:
    - Modes of n/pMOS operation and associated current models.
    - 2nd order effects: e.g., body effect, channel length modulation
    - Apply MOS devices in circuit: guess mode, solve KCL/KVL, check, change guess and repeat if necessary.
    - Inverter circuit definitions and analysis (e.g., V_L, V_{IH}, NM_L,…)
    - Simple logic gates (NAND, NOR).
- Office hours this week: today 2-3pm in EE218.

Complex Logic Design

- Write output in sum-of-product form, e.g.

$$Y = \overline{AB + CDB}$$

- Place NMOS switches
  - AND => series
  - OR => parallel
- Design *W*/*L* ratios



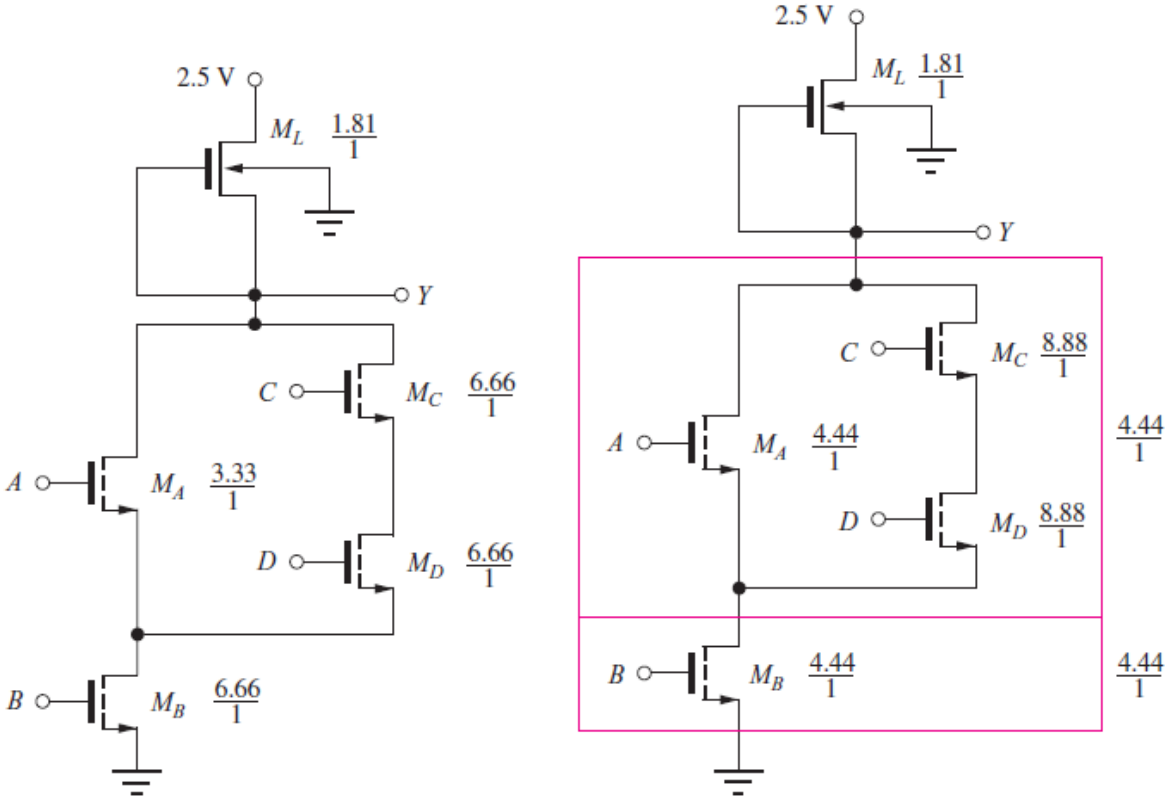
Complex Logic Gate Transistor Sizing

- Two ways to find the W/L ratios of the switching transistors

1) Using the worst case (longest) path and choosing the W/L ratio such that the total R_{on} of the path is equal to that of M_S in the reference converter

2) Partitioning the circuit into series sub-networks, and make the equivalent on-resistances equal

Find *W*/*L* ratios



$$Y = \overline{AB + CDB} = \overline{(A + CD)B}$$

Static Power Dissipation

- Static Power Dissipation is the average power dissipation of a logic gate when the output is in both the high and low states

$$P_{av} = \frac{V_{DD} I_{DDH} + V_{DD} I_{DDL}}{2}$$

- I_{DDH} = current in the circuit for $v_O = V_H$
- I_{DDL} = current in the circuit for $v_O = V_L$

- Since $I_{DDH} = 0$ A for $v_O = V_H$: $P_{av} = \frac{V_{DD} I_{DDL}}{2}$

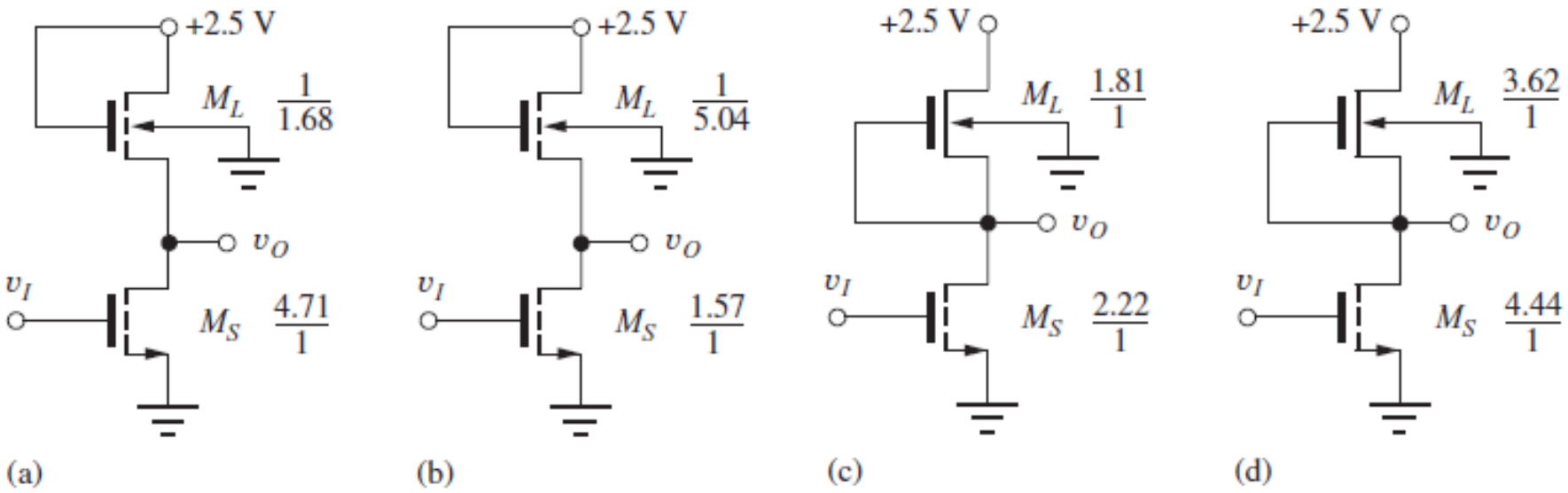
- However, worst case is: $P_{av} = V_{DD} I_{DDL}$

Power Scaling in NMOS Logic

- By changing the W/L of the load and switching transistors, it is possible to scale the power level up or down without disturbing V_H and V_L levels.

$$P \propto i_D \propto \left(\frac{W}{L}\right)$$

Power Scaling in MOS Logic



a) Original Saturated Load Inverter
b) Saturated Load inverter designed to operate at 1/3 the power
c) Original Depletion-Mode Inverter
d) Depletion-mode inverter designed to operate at twice the power

